FIG. 1

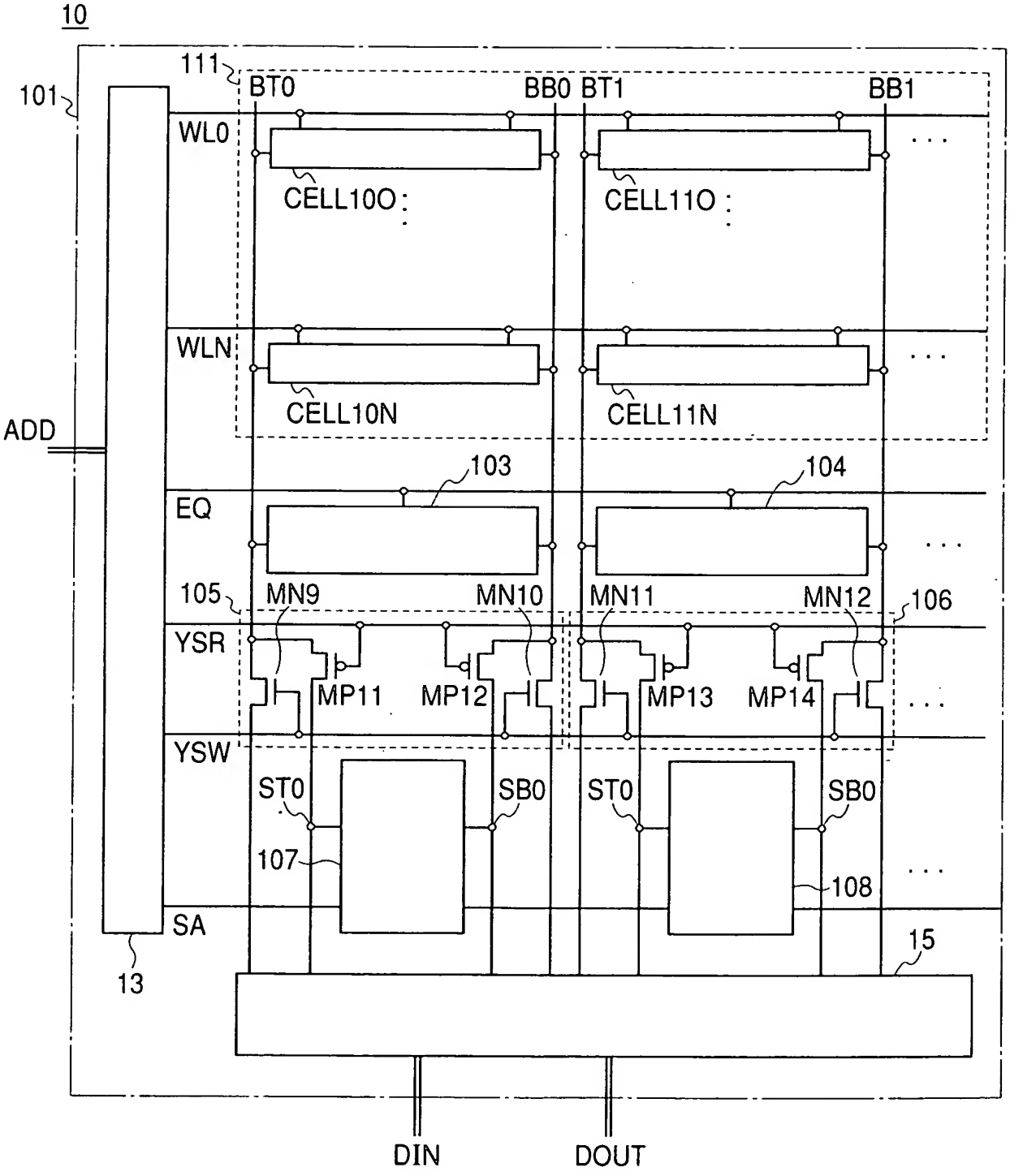
10
111
101
BT0
BB0
BT1
BB1
WL0
CELL10O
CELL11O
WLN
CELL10N
CELL11N
ADD
103
104
EQ
105
MN9
MN10
MN11
MN12
106
YSR
MP11
MP12
MP13
MP14
YSW
ST0
SB0
ST0
SB0
107
108
SA
13
15
DIN
DOUT

FIG. 2

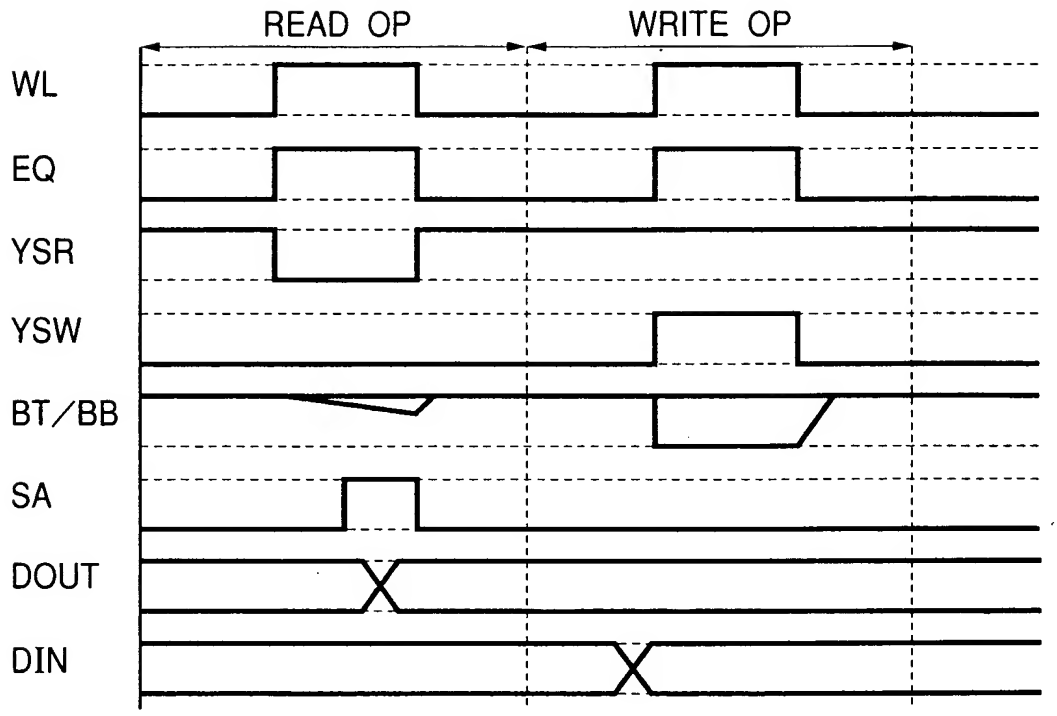

FIG. 3

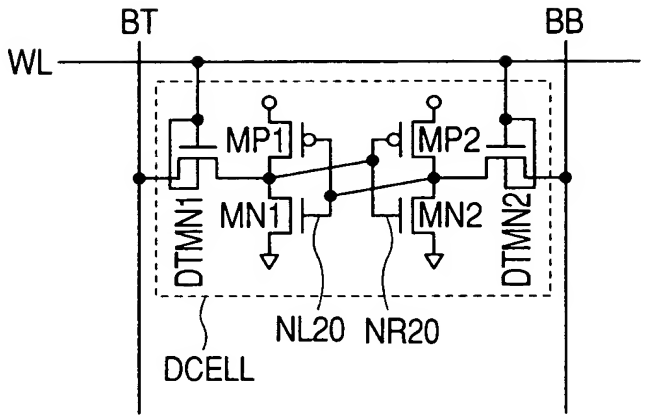
BT
BB
WL
MP1
MP2
DTMN1
MN1
MN2
DTMN2
NL20
NR20
DCELL

FIG. 4

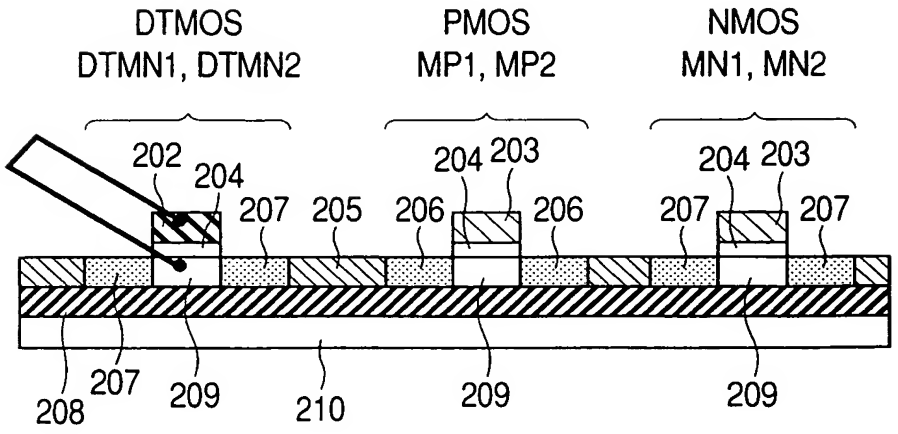
DTMOS
DTMN1, DTMN2
PMOS
MP1, MP2
NMOS
MN1, MN2
202
204
207
205
206
204
203
206
207
204
203
207
208
207
209
210
209
209

FIG. 5

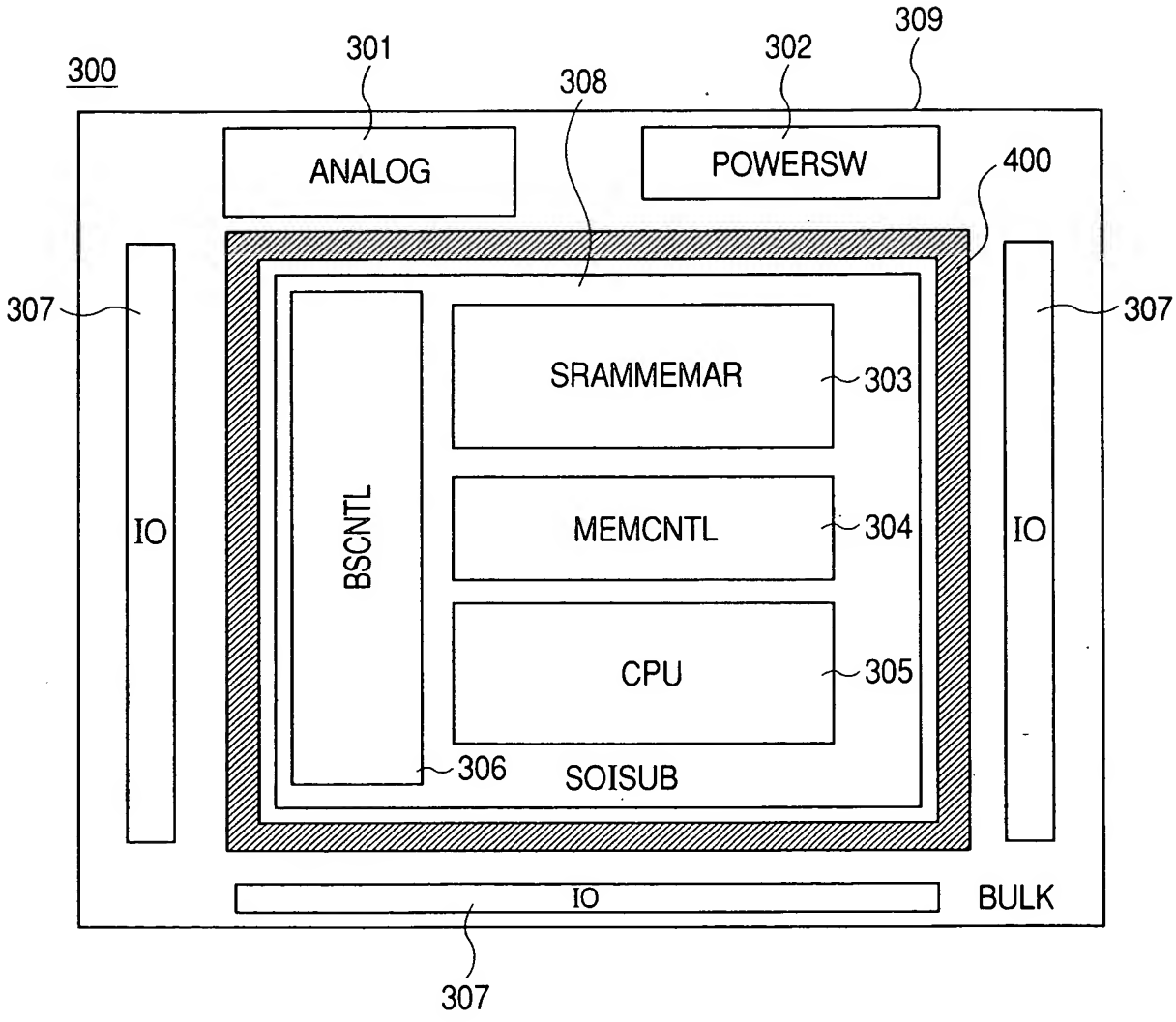
300
301
302
309
308
ANALOG
POWERSW
400
307
307
IO
IO
BSCNTL
SRAMMEMAR
303
MEMCNTL
304
CPU
305
306
SOISUB
IO
BULK
307

FIG. 6

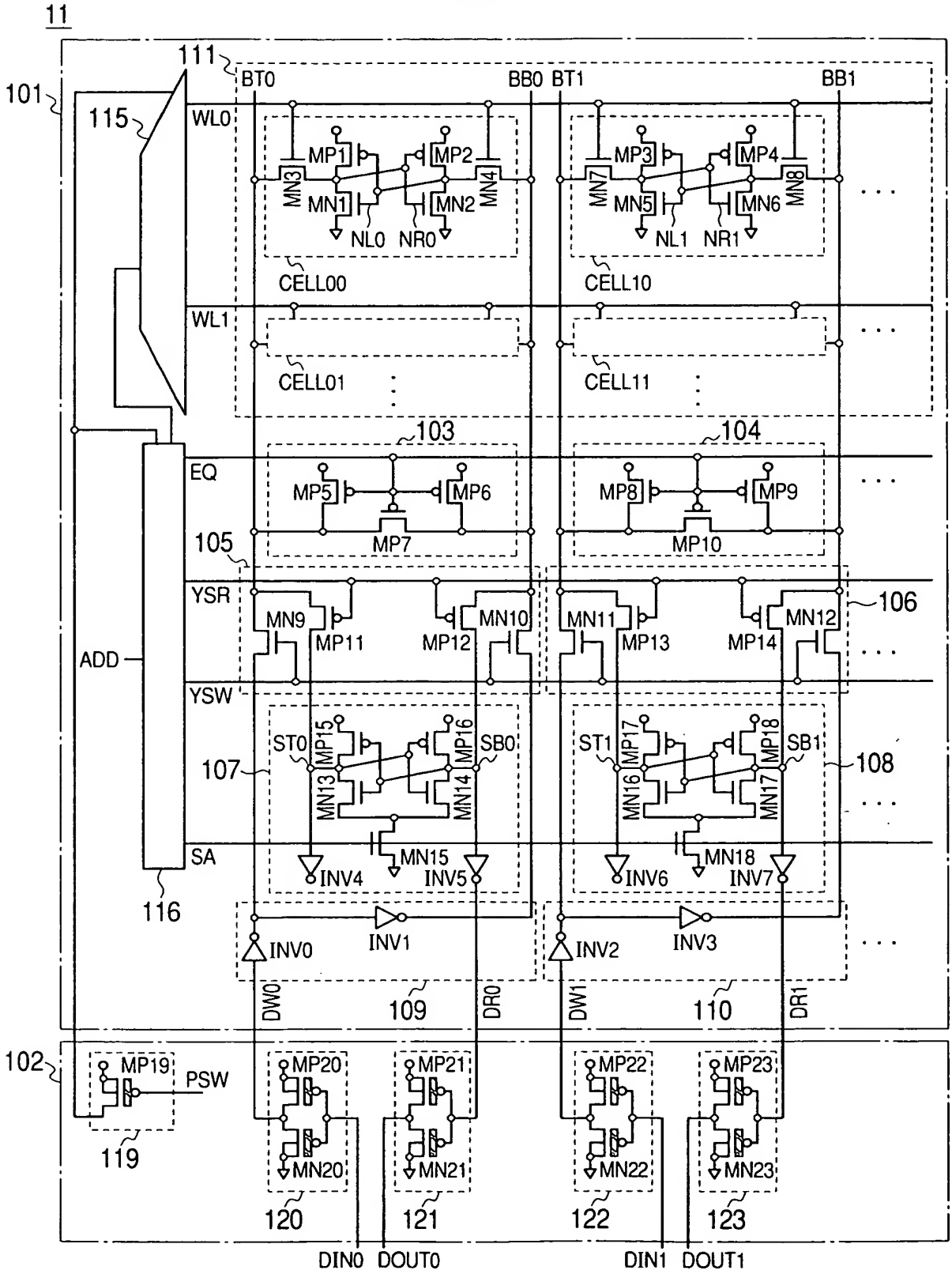
11
111
101
115
BT0
BB0
BT1
BB1
WL0
WL1
MP1
MP2
MP3
MP4
MN1
MN2
MN3
MN4
MN5
MN6
MN7
MN8
NL0
NR0
NL1
NR1
CELL00
CELL10
CELL01
CELL11
103
104
EQ
MP5
MP6
MP7
MP8
MP9
MP10
105
YSR
MN9
MN10
MN11
MN12
MP11
MP12
MP13
MP14
106
ADD
YSW
ST0
SB0
ST1
SB1
MP15
MP16
MP17
MP18
MN13
MN14
MN16
MN17
107
108
SA
MN15
MN18
INV4
INV5
INV6
INV7
116
INV0
INV1
INV2
INV3
DW0
DR0
DW1
DR1
109
110
102
MP19
PSW
119
MP20
MP21
MP22
MP23
MN20
MN21
MN22
MN23
120
121
122
123
DIN0
DOUT0
DIN1
DOUT1

FIG. 7

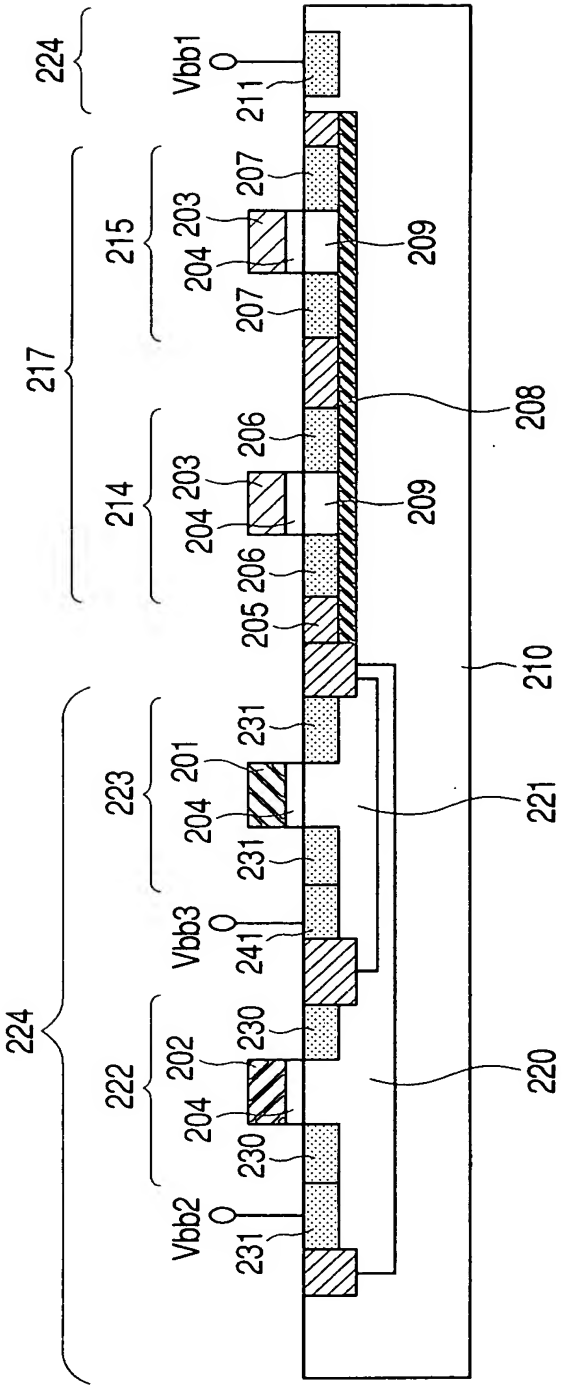
224
Vbb1
211
207
215
203
204
209
207
217
208
214
206
203
204
209
206
205
210
231
201
223
204
221
231
Vbb3
241
224
230
202
222
220
204
230
Vbb2
231

FIG. 8

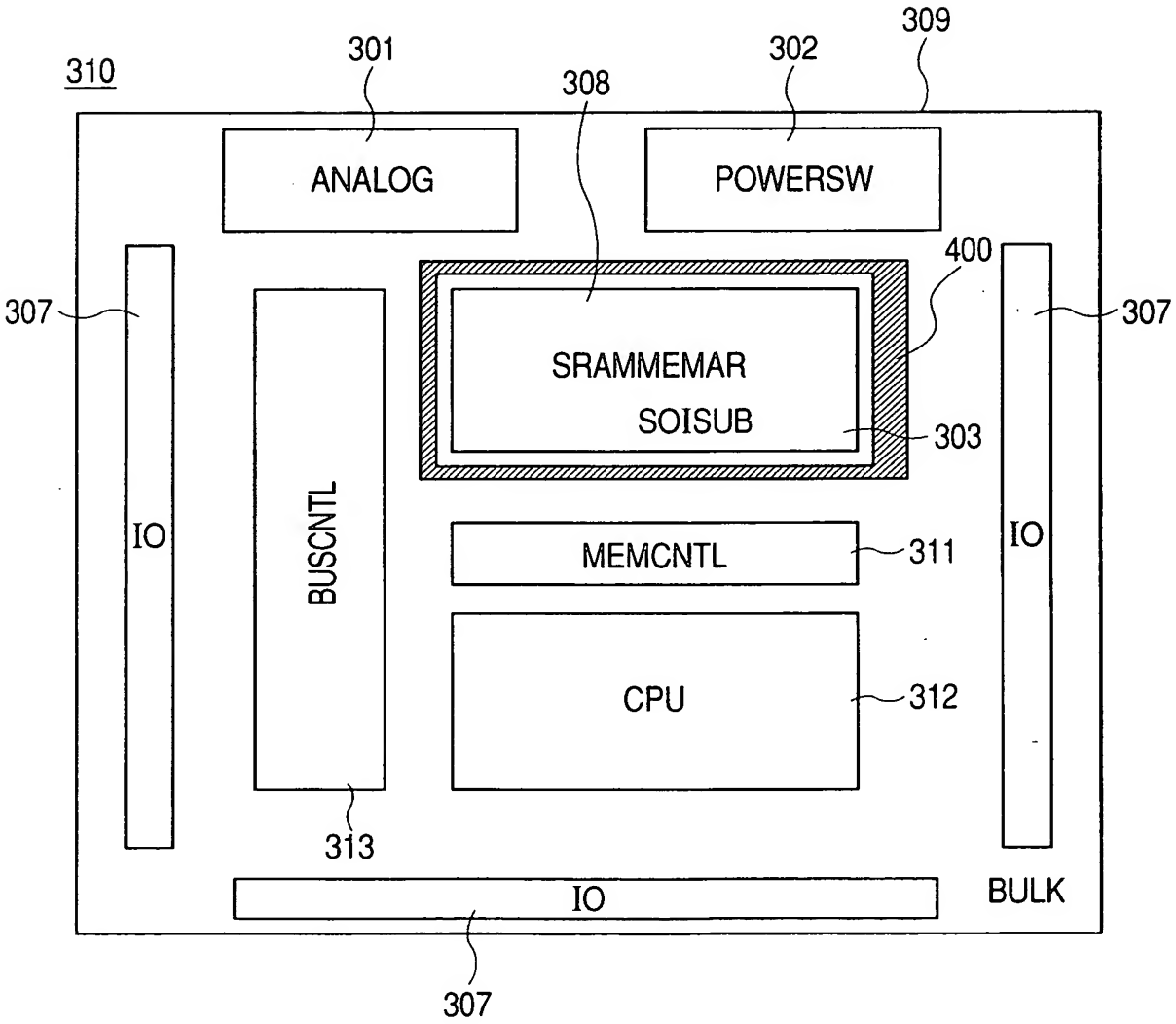
310
301
308
302
309
ANALOG
POWERSW
400
307
SRAMMEMAR
SOISUB
303
307
IO
BUSCNTL
MEMCNTL
311
IO
CPU
312
313
IO
BULK
307

FIG. 9

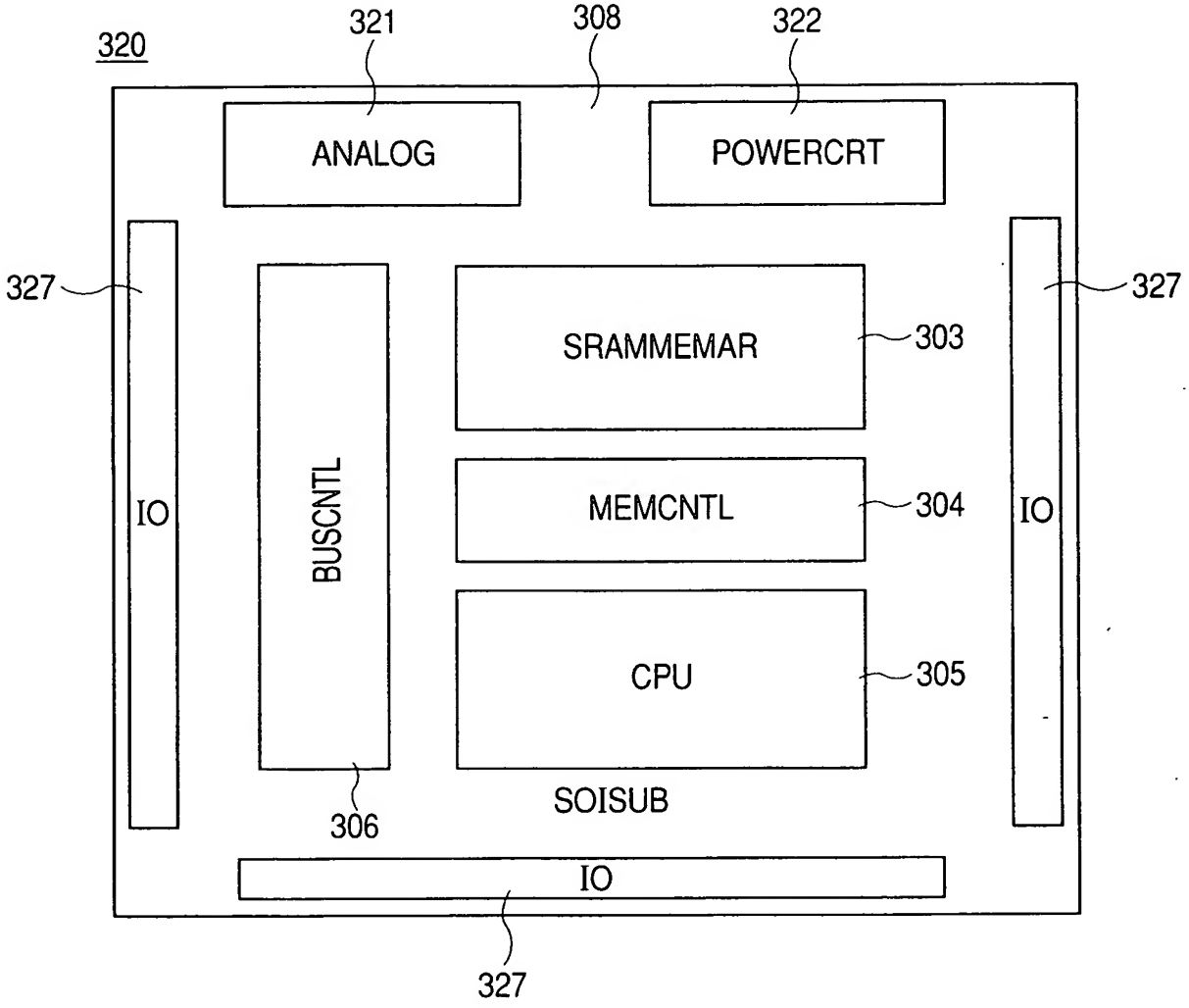
320
321
308
322
ANALOG
POWERCRT
327
IO
BUSCNTL
SRAMMEMAR
303
MEMCNTL
304
CPU
305
IO
327
306
SOISUB
IO
327

FIG. 10

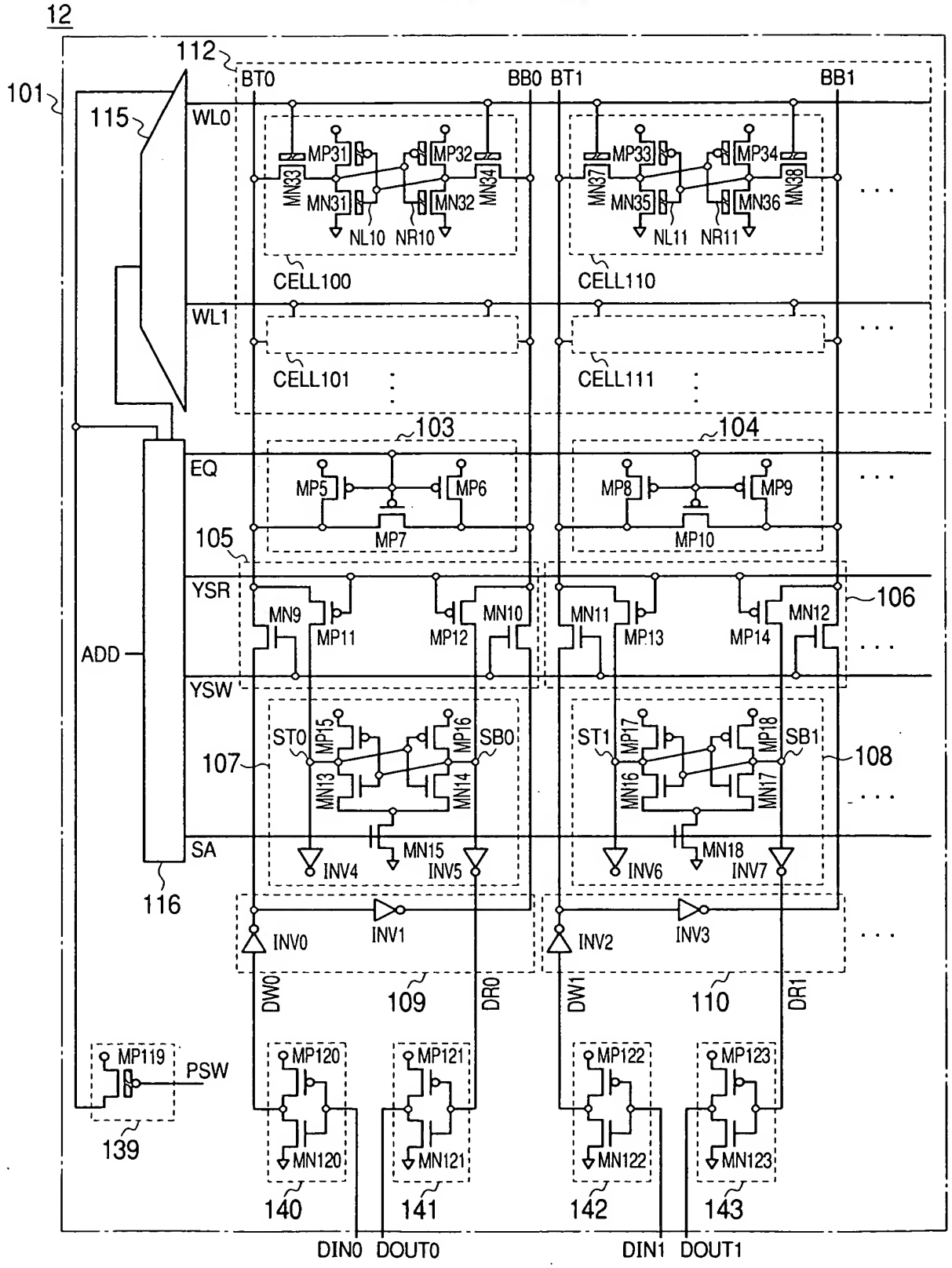
12
112
101
115
BT0
BB0
BT1
BB1
WL0
WL1
MP31
MP32
MP33
MP34
MN31
MN32
MN35
MN36
MN33
MN34
MN37
MN38
NL10
NR10
NL11
NR11
CELL100
CELL110
CELL101
CELL111
103
104
EQ
MP5
MP6
MP7
MP8
MP9
MP10
105
YSR
MN9
MP11
MP12
MN10
MN11
MP13
MP14
MN12
106
ADD
YSW
ST0
MP15
MP16
SB0
ST1
MP17
MP18
SB1
107
108
MN13
MN14
MN16
MN17
SA
MN15
MN18
INV4
INV5
INV6
INV7
116
INV0
INV1
INV2
INV3
DW0
109
DR0
DW1
110
DR1
MP119
PSW
MP120
MP121
MP122
MP123
139
MN120
MN121
MN122
MN123
140
141
142
143
DIN0
DOUT0
DIN1
DOUT1

FIG. 11

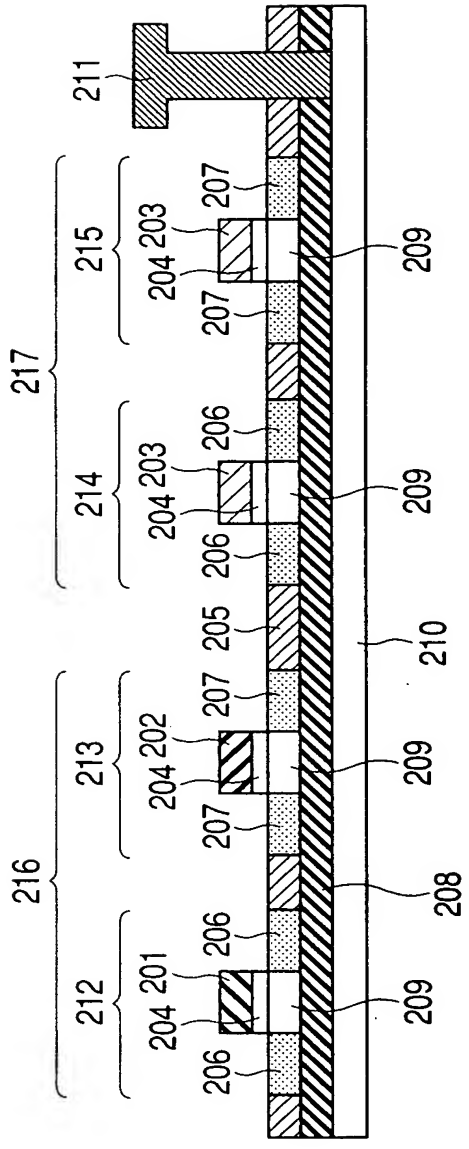
211
217
215
214
213
216
212
207
203
204
209
206
205
210
202
201
208

FIG. 12

SOISUB		HIGHSPEED					STANDARD				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	SiGe	P	○	−0.3	SOI	SiGe	P	3V	−0.3
	NMISFET	SOI	SiGe	P	○	0.3	SOI	SiGe	P	3V	0.3
SRAM	PMISFET	SOI	SiGe	P	○	−0.3	SOI	Poly-Si	N	3V	−1.0
	NMISFET	SOI	SiGe	P	○	0.3	SOI	Poly-Si	P	3V	0.6

SOISUB		STANDARD					LOWPOWER				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	×	−0.8
	NMISFET	SOI	Poly-Si	P	3V	0.6	SOI	Poly-Si	P	×	0.8
SRAM	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	×	−0.8
	NMISFET	SOI	Poly-Si	P	3V	0.6	SOI	Poly-Si	P	×	0.8

HYBRIDSUB		HIGHSPEED					STANDARD				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	SiGe	P	○	−0.3	SOI	SiGe	P	3V	−0.3
	NMISFET	SOI	SiGe	P	○	0.3	SOI	SiGe	P	3V	0.3
SRAM	PMISFET	SOI	SiGe	P	○	−0.3	SOI	Poly-Si	N	3V	−1.0
	NMISFET	SOI	SiGe	P	○	0.3	SOI	Poly-Si	P	3V	0.6
IO/Analog/SW		BULK	-	-	-	ANY	BULK	-	-	-	ANY

HYBRIDSUB		STANDARD					LOWPOWER				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	BULK	-	-	-	ANY	BULK	-	-	-	ANY
	NMISFET	BULK	-	-	-	ANY	BULK	-	-	-	ANY
SRAM	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	×	−0.8
	NMISFET	SOI	SiGe	P	NONE	0.5	SOI	Poly-Si	P	×	0.8
IO/Analog/SW		BULK	-	-	-	ANY	BULK	-	-	-	ANY

FIG. 13

		HIGH SPEED 300MHz～ Vdd<1.0V	STANDARD 100MHz～300MHz Vdd≒1.0V	LOW POWER ～100MHz Vdd>1.0V
Logic	PMOSVT	−0.3V～−0.1V	−0.4V～−0.2V	−0.9V～−0.7V
	NMOSVT	0.1V～0.3V	0.2V～0.4V	0.7V～0.9V
SRAM	PMOSVT	−0.5V～−0.3V	−1.0V～−0.8V	−0.9V～−0.7V
	NMOSVT	0.2V～0.4V	0.4V～0.6V	0.7V～0.9V

FIG. 14

GATE MAT	Poly-Si		SiGe	
GATE IMP	P	N	P	N
PMOS Vto	+0.2V	−0.8V	−0.1V	−0.8V
NMOS Vto	+0.8V	−0.2V	0.5V	−0.2V

FIG. 15

	ELE	BULK	FD-SOI
Vbbb	LVthMOS + VBBBCRT	EFFECT IS LOW UNDER 100nm	EFFECT EVEN UNDER 100nm
Vbbf	HVthMOS + VBBFCRT	EFFECT IS LOW AT HIGH TEMPERATURE LEAK CURRENT IS LARGE	HIGH TEMPERATURE OPERATION AVAILABLE, SMALL LEAK CURRENT, ON CURRENT LARGE
Vbbact	VthMOS + MNTCRT + VLTCRT	WITH ABOVE REASONS, CORRECTIONS FOR VTH DISPERSION IS NOT EFFECTIVE	EFFECTIVE UNDER 100nm & HIGH TEMPERATURE

FIG. 16

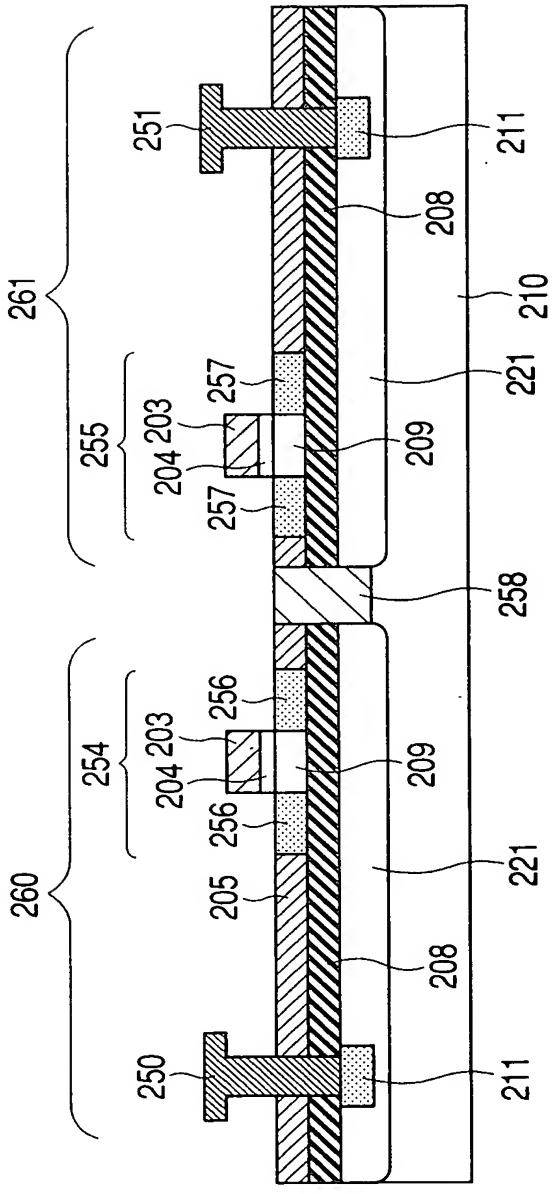
261
255
254
260
251
250
211
208
210
221
257
203
204
209
256
205
258

FIG. 17

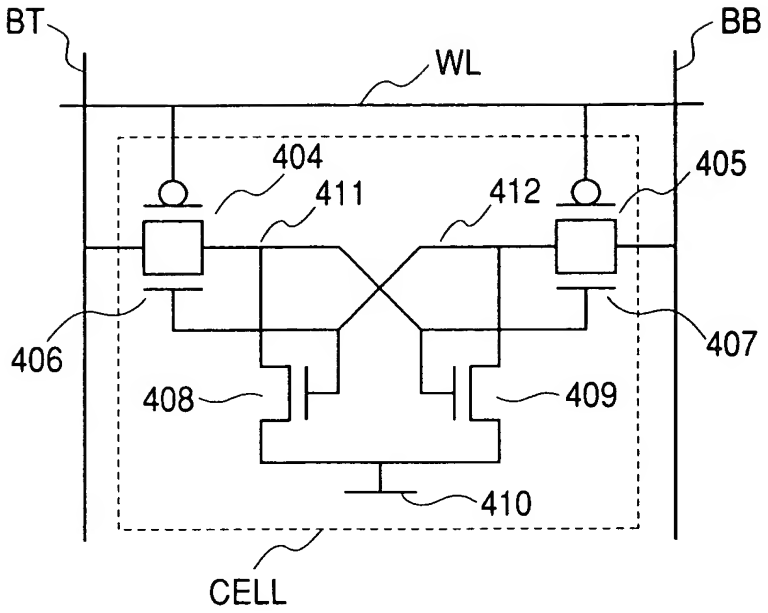
BT
BB
WL
404
411
412
405
406
407
408
409
410
CELL

FIG. 18

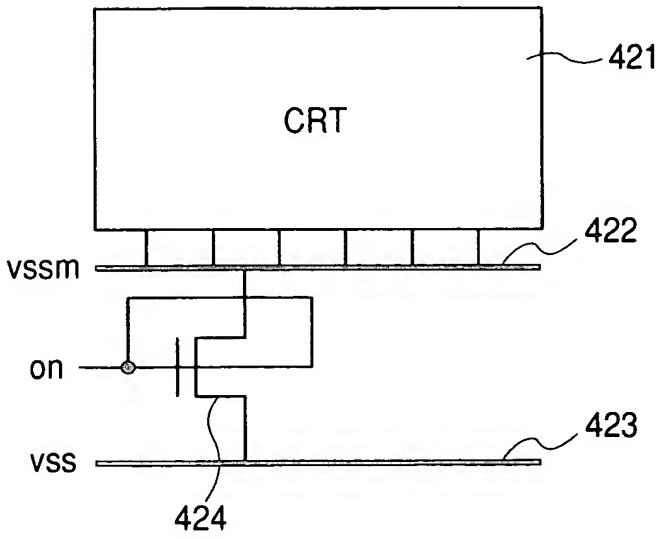
421
CRT
422
vssm
on
423
vss
424

FIG. 19